Troubleshooting High-Speed Source Synchronous Systems

▶ Choose the Right Logic Analyzer Clocking Mode

Introduction

High-speed synchronous digital buses are changing in many ways. Not only are they increasing in speed, but also they are changing in the way the data is transferred. Gone are the days when data was transferred on the rising edge of the main bus clock. In the never-ending pursuit of improved data throughput, emerging synchronous digital buses send data multiple times per cycle using a diverse array of clocking schemes. Synchronous data transfers are becoming ever more common in emerging computing, networking, and communications architectures. With this trend comes an urgent requirement for efficient digital acquisition tools that can assist engineers in their troubleshooting and verification work.

To keep pace with the trend toward high-speed synchronous digital buses, today's logic analyzers must offer great flexibility in clocking and triggering. They must be able to capture data without the use of external devices to "pre-condition" the data before it enters the instrument itself. To meet the needs of digital designers confronting time-to-market and technical challenges, logic analyzers need to have complex synchronous clocking capabilities built into the data acquisition system's front end.

The Tektronix TLA700 Series logic analyzers include a wealth of clocking capabilities to address all of the data transfer methods outlined above, including source-synchronous clocking.

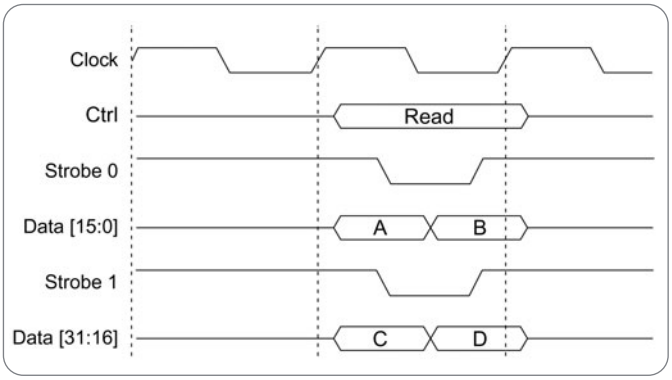
This application note will explain how to use these specialized clocking features to acquire data from complex high-speed synchronous data buses, including source-synchronous buses.

Challenges in Capturing Today's High Speed Digital Buses

In their pursuit of ever-increasing data throughput in PCs, servers, and communications equipment, designers have learned that simply increasing the base clock rate is no longer enough to achieve higher bandwidth. Departing from basic edge-triggered clocking, in which data transfers on the leading edge of each cycle's clock pulse, digital architects have devised a number of alternative approaches:

- One bit of data transfers on two edges (leading and trailing) in each cycle
- Two bits of data transfer on one edge in each cycle (double-pumped data)
- Two bits transfer on two edges in each cycle (quad-pumped data)
- "Multiple" bits transfer with a special strobe signal rather than a clock

The latter method is known as source-synchronous clocking architecture. This approach is gaining wider acceptance and will be the focus of some application examples later in this document. In a typical source-synchronous transaction, the transmitting device sends data multiple times within each cycle, along with a strobe associated with each data group. The receiving device uses this strobe to latch the data, then resynchronizes the data to the master or common clock. Some DDR memory buses and front side buses, as well as AGPnX graphics cards use this technique. DDR memories have an equivalent data transfer rate up to 800 MT/s and front side buses have an equivalent transfer rate up to 533 MT/s. Figure 1 shows the timing relationships among the signals involved in a typical source synchronous data transfer.



► ***Figure 1.*** *Typical source synchronous data transfer.*

Another method of improving data bandwidth is to reduce the number of data channels, multiplex the data, and increase the synchronous clock frequency substantially. To achieve these higher clock frequencies, the data is sent differentially and at reduced signal amplitudes. High-speed buses implementing this scheme include Rapid I/O, whose data transfer rates range from 100 MT/s to 2 GT/s, and HyperTransport, with data rates ranging from 400 MT/s to 2 GT/s.

The tools needed to capture data from the foregoing types of buses consist primarily of logic analyzers and oscilloscopes. With proper connections to the bus and observing high-speed digital design rules, data can be presented to the logic analyzer or oscilloscope with good signal integrity.

While most of today's logic analyzers are capable of capturing this high-speed data, there is almost always a requirement for an external pre-processor on the front end to "pre-condition" the data so the analyzer can interpret the newer data protocols. Pre-conditioning is necessary because the logic analyzer lacks the complex clocking capabilities needed to interpret the high speed synchronous 2X, 4X and source synchronous data protocols that are now prevalent in today's digital buses.

Pre-conditioning tools take up valuable lab space and are time-consuming to setup. They also latch the data, making it impossible to see the raw timing of the digital or analog signals. This makes it difficult to find timing and analog problems.

Oscilloscopes are also powerful debug tools, but their channel count is limited. It can be very time-consuming to find the four critical signals that will reveal an elusive timing bug. But the oscilloscope is very good at finding analog integrity-related problems, if the instrument has direct access to the data bus. This capability is now

Clocking Mode	Measurement/Application	Typical System under Test
1X Internal (asynchronous)	Waveform views, not synchronized with SUT events	General-purpose digital measurements with clock rates to 500 MHz
2X Internal (asynchronous)	Waveform views, not synchronized with SUT events	General-purpose digital measurements with clock rates to 1 GHz
4X Internal (asynchronous)	Waveform views, not synchronized with SUT events	General-purpose digital measurements with clock rates to 2 GHz
1X External (synchronous) One edge	Waveform and listing views, synchronized with SUT events	FSB, conventional edge-clocked devices
1X External (synchronous) Two edges	Acquisition double or quad-pumped data (requires demux)	AGP2X (double-pumped) AGP4X (quad-pumped)
1X External (synchronous) Two edges ("quad-pumped")	Slower quad-pumped data acquisition using demux	Quad-pumped FSB architectures
2X External (synchronous) One edge	Fast acquisitions with two data bits per cycle clocked by one edge	Rambus memory architecture
2X External (synchronous) Two edges	Acquisition of two data bits per cycle, one from each clock edge	Double Data Rate (DDR) memory devices and buses
4X External (synchronous) Two edges ("quad-pumped")	Fastest quad-pumped acquisition (to 1.25 Gb/s)	RapidIO, HyperTransport, other high-speed comm buses
Source Synchronous Edge-independent	Acquisition of strobe-dependent data rather than clocked data	DDR, AGP2X, AGP4X, AGP8X

► ***Table 1.*** *Available clocking modes for the Tektronix TLA700 Series logic analyzers.*

available with the iLinkTM Tool Set capability that couples TLA700 Series logic analyzers with TDS5000/6000/7000 Series oscilloscopes. Many oscilloscope models can be interfaced to TLA700 Series logic analyzers to acquire signals through the logic analyzer probes and display time-correlated analog waveform views on the logic analyzer display.

Advanced Clocking Features Support Asynchronous and Synchronous Bus Acquisitions

The Tektronix TLA700 Series logic analyzer with TLA7Axx advanced logic acquisition module provides a feature set that addresses the all of the prevalent high-speed synchronous acquisition requirements. Table 1 equates the full range of TLA700 Series logic analyzer clocking modes with the device clocking approaches discussed earlier. Internal (asynchronous) clocking modes are used for timing acquisitions only and are not covered in this document, but are included here for the sake of comprehensiveness.

The TLA7Axx setup menu in Figure 2 shows a pull-down menu with the available clocking mode selections.

Characteristics of the TLA7Axx Clocking Modes

Internal Clocking (1X, 2X, 4X)

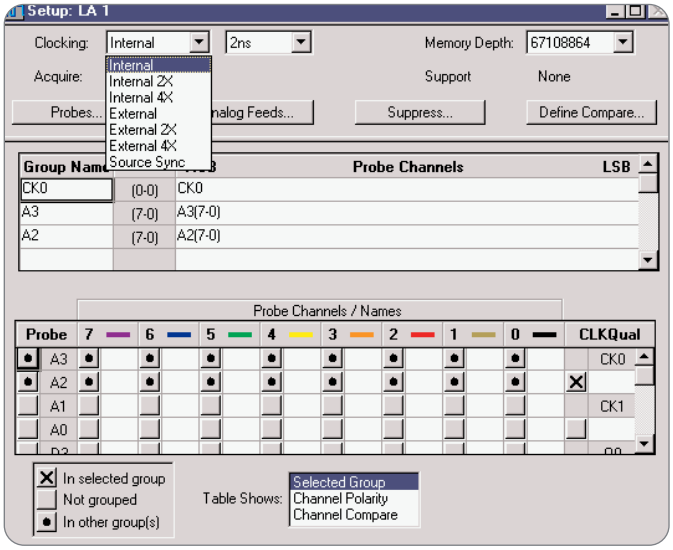
Each internal (asynchronous) clocking mode offers a unique combination of clock rate, channel count, and memory depth. 1x internal clocking, for example, is ideal for capturing data from busses and devices that are relatively “slow” but very wide. In the 1x mode, the logic analyzer can acquire data on up to 136 channels (per acquisition module) at once. In contrast, 4x internal clocking is best suited for work with very fast, narrower busses that may generate many millions of data cycles in normal operation. The 8 GHz MagniVu™ timing feature is always active, irrespective of the clock mode.

1X Internal

- Default internal clock rate is 500MHz (2 nsec)
- Maximum acquisition depth: up to 64M samples for very long timing acquisitions
- Sample clock can be user-adjusted from 2 nsec to 50 msec

2X Internal

- Equivalent internal clock rate is 1 GHz (1 nsec)
- Memory depth is doubled to 128M samples
- Two-way demultiplexing of the data cuts channel width in half
- Data display provides a "normalized" view of the data
- EasyTrigger provides a variety of trigger templates to simplify trigger setup



▶ ***Figure 2.*** *TLA7Axx Setup menu with available clocking modes.*

4X Internal

- Allows the sampling of the data at clock rates up to 2 GHz (500 psec)
- Memory depth extends to 256M samples
- Four-way demultiplexing technique supports up to 136 channels by merging four acquisition modules.
- Data display provides a "normalized" view of the data
- EasyTrigger provides a variety of trigger templates to simplify trigger setup

External Clocking (1X, 2X, 4X)

External (synchronous) clocking is the key to acquiring data most efficiently; each sample equates to a specific clock event on the bus and the resulting data can be used to reconstruct detailed listings of bus activity as well as timing diagrams. While massive memory depth still a desirable attribute, it is less critical than in the internal clocking modes because only events are recorded—not the passage of time between them.

Like the internal clocking modes, there are three basic external clocking modes.

1X External (Synchronous)

- Clock rates up to 450 MHz with full channel count
- Effective maximum data rate is 450 Mb/s

2X External (Synchronous)

- Clock rates up to 800 MHz with channel count reduced by half. A special 2X synchronous circuit on the logic analyzer’s front end enables this function
- Effective maximum data rate is 800 Mb/s

4X External (Synchronous)

- Maximum clock speed is 625 MHz
- Channel count depends on multiplexing scheme used
- Effective maximum data rate is 1250 Mb/s

Overview of the Clocking Menus

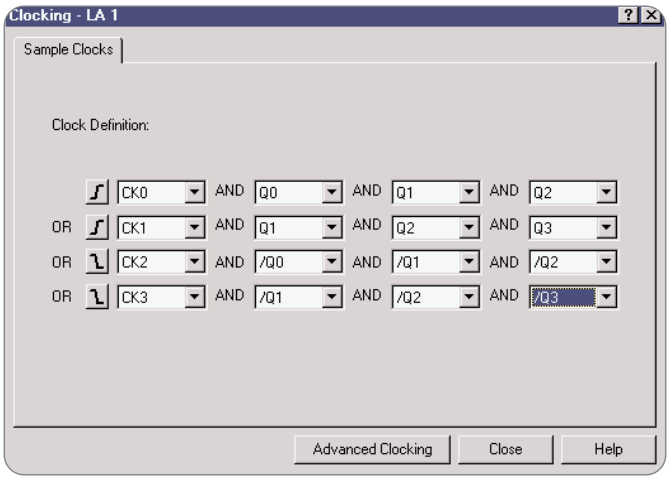
Figure 3 shows an example of the basic clocking menu for the External 1X clocking mode. The clocking equation can use up to four OR'ed clocks, and each of these clocks may be AND'ed with up to three qualifiers.

Beyond the basic clocking capabilities of the TLA7Axx module there are advanced clocking features, accessed via the "Advanced Clocking" button at the bottom of the window. Figure 4 shows the resulting display: the Advanced External 1X Sample Clocks window. The same Sample Clocks submenu exists, but a second Sample Clock choice is available on a pull-down, allowing you to set up two different sample clock equations. In Figure 4, Sample Clock 1 is the master clock.

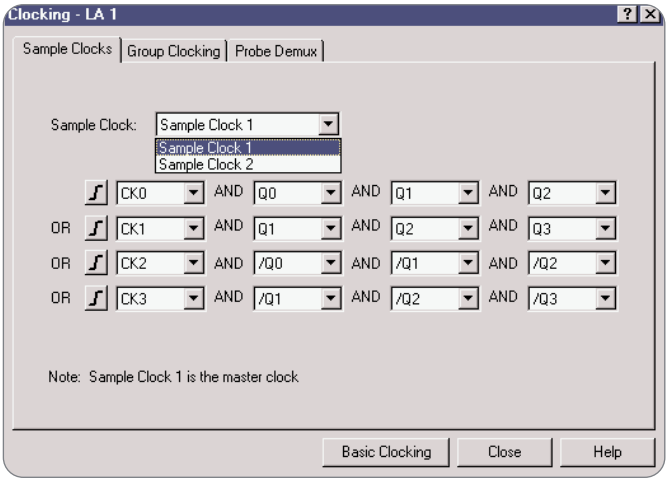
Looking again at Figure 4, note that two additional tabs—Group Clocking and Probe Demux—have appeared. Clicking the Group Clocking tab produces the screen shown in Figure 5. Here you can define "Group" information that includes the sample clocks associated with the group, the number of clock pipeline delays (up to seven) for the group, particular channel group, and the setup/hold sample window.

The 625 psec setup/hold sample window, adjustable in 125 psec steps, ranges from +16.125 ns setup to +8.375 ns hold relative to the selected clock edge. You may select the maximum synchronous clock speed available or you may choose slower speeds, either 235 MHz or 120 MHz. This clocking mode is useful for capturing complex buses with large channel counts and multiple data qualifiers.

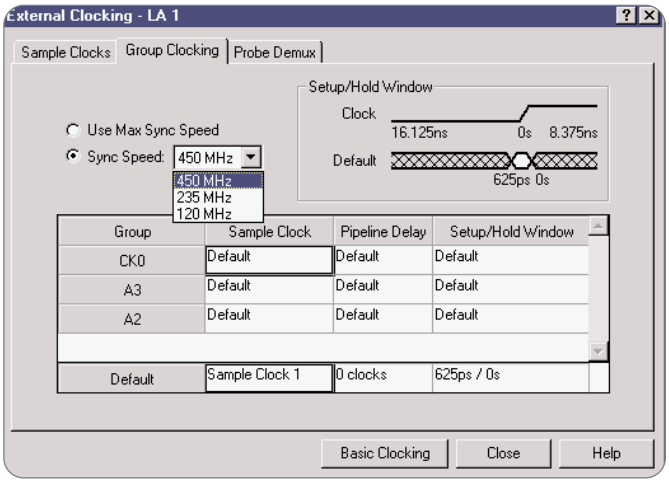
The last tab on the External Clocking window brings up the Probe Demux submenu, Figure 6. Here you can individually select which channel groups to demultiplex (either two-way or four-way). In addition there are buttons to select all or none, respectively.



► ***Figure 3.*** *External 1X Basic Clocking submenu.*



► ***Figure 4.*** *Advanced External 1X Sample Clocks submenu.*



► ***Figure 5.*** *Advanced External 1X Group clocking submenu.*

External 2X

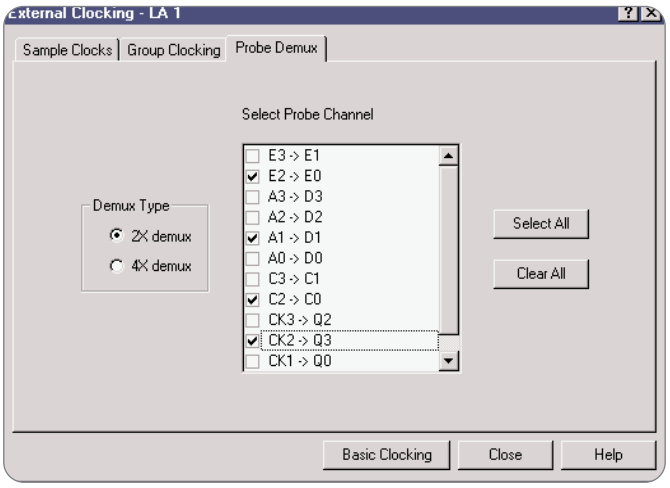
External 2X Clocking (Figure 7) is a multiplexed format that supports the TLA7Axx module's highest possible clock rates. Edge spacing within any one signal can be as little as 1.25 ns. In this mode you can select up to four different clock sources. Each source can be set to respond the rising edge, the falling edge, or both. Here the 625 psec setup/hold sample window ranges from +8 ns setup to +8.375 ns hold relative to the selected clock edge. Using the External 2X clocking mode you might, for example, sample a set of multiplexed data (double pumped data) at two different times with synchronous clock rates up to 800 MHz and double data rates up to 800 Mb/s.

Figure 8 shows the advantage of external 2X clocking when compared to 1X clocking. Using standard 1X clocking on the 800 MHz SUT in the uppermost set of waveforms, exactly half of the data is lost because samples are taken at 2.5 ns intervals rather than 1.25 ns. With 2X clocking, two groups work together to sample twice as frequently. The data in D3 is meaningless but A3 contains every bit of data the SUT produces on the A3 channel (similarly, the 4X mode combines the resources of four channels to support full acquisition on one channel). If it is necessary to see the true output of D3 as well, then it cannot be paired with A3 like this; both must be separately paired with spare channels that can share their sampling resources.

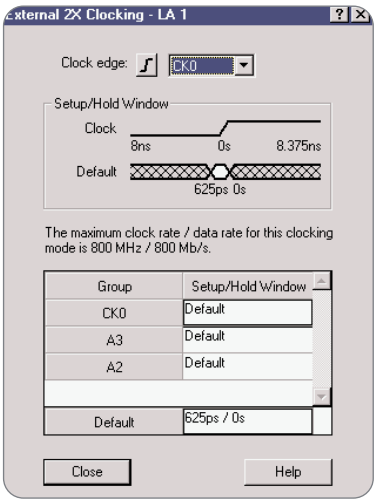
A second method of External 2X clocking is aimed at DDR requirements. Here, the data is captured on both edges of the clock—rising and falling. The maximum clock rate is equal to the base sync speed of the TLA7Axx module—450 MHz. To implement External 2X DDR clocking, you need only make the proper choices in the Clocking menu, as shown in Figure 16 later in this document. Note that the "Clock edge" button (near the CKØ pull-down) shows two edges active, in contrast to the standard 2X clocking menu shown earlier.

In the 2X DDR mode, the clock duty cycle does not have to be symmetrical but it does have to be free of unwanted transients and aberrations. Should a random glitch get into the signal, it will register as a valid edge and cause erratic misalignments of the acquisition data.

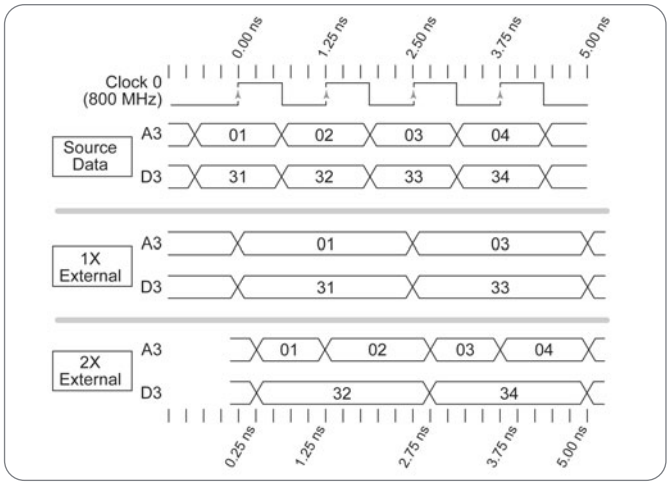
The next step up is External 4X Clocking. Here you have the choice of up to four different clock sources, each one using either the rising or falling edge. For this clocking mode, the 625 psec setup/hold sample window ranges from +8 ns setup to +7.625 ns hold relative to the selected clock edge.



▶ ***Figure 6.*** *Advanced External 1X Demux submenu.*



▶ ***Figure 7.*** *External 2X Clocking submenu.*

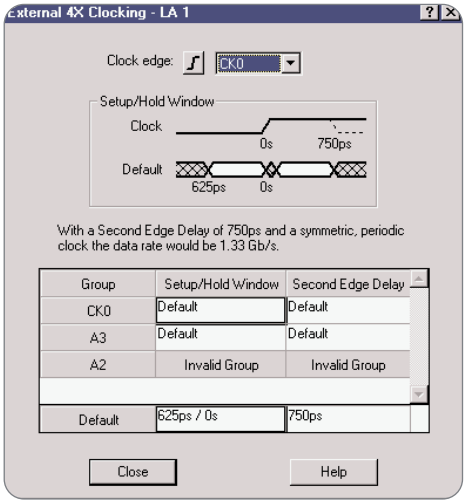


▶ ***Figure 8.*** *Comparison of External 2X timing results with a basic1X acquisition.*

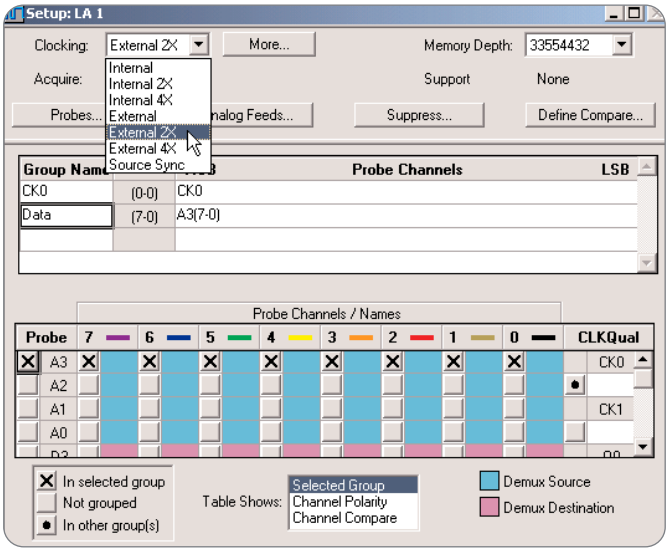
In the External 4X Clocking submenu there is a four-way demux and a second edge delay to program. The first setup/hold window adjustment is relative to the rising or falling edge of the user-selected clock. The second edge delay adjustment is the delay after the first clock edge. Using the External 4X Clocking mode you can sample a set of multiplexed data (quad pumped data) at four different times up to 625 MHz and quad data rates up to 1.25 Gb/s. Figure 9 shows the External 4X Clocking submenu.

As we have seen in this overview of clocking modes, each mode matches the needs of a particular SUT clocking architecture. The TLA700 Series logic analyzer has kept pace with the needs of emerging bus architectures, offering a steady stream of enhancements in speed, clocking options, triggering features, and bus support since its introduction.

Selecting the right acquisition mode for your SUT is a matter of assessing the frequency and data rate requirements, plus the synchronization functions ranging from common leading-edge-clocked to quad pumped and source sync. The balance of this document is devoted to examples that summarize the steps needed to implement these external clocking modes: 1X, 2X, 4X, and source synchronous, with particular emphasis on the latter mode.



▶ ***Figure 9.*** *External 4X Clocking submenu.*



▶ ***Figure 10.*** *2X External Mode Setup page.*

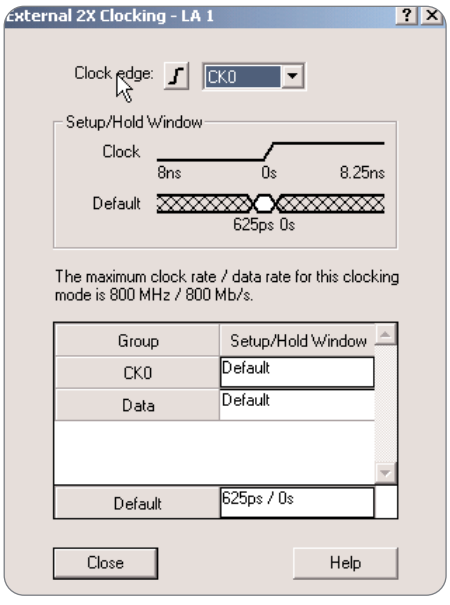
Step-by—Step Application Examples: Clock-Synchronous Buses

2X External Clocking

The typical target device for the 2X External mode, also known as the Fast Clock mode, is one that uses a single edge to clock data at very high speeds—up to 800 MHz.

Begin by selecting “2X External” on the “Clocking” pull-down menu on the Setup page as in Figure 10. Designate the clock and data Probe Channels appropriately to match the probes and pins you have connected to your device.

Next, go to the “Clock edge” pull-down in the Clocking window (Figure 11). Select CK0 from the available signal names previously entered on the Setup page, and using the button next to the pull-down, choose the single rising. Edit any Setup/Hold values as needed, or accept the defaults.



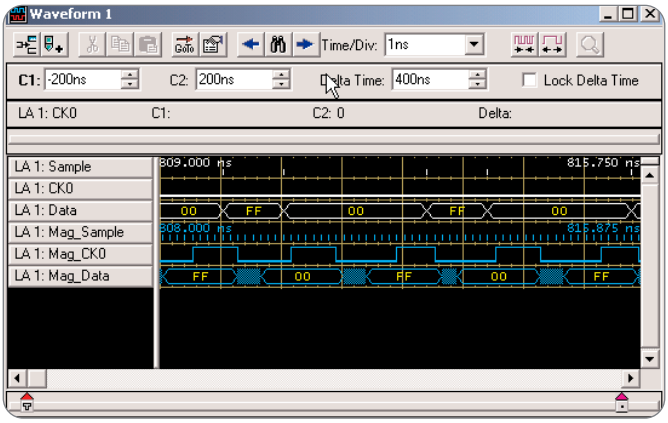
▶ ***Figure 11.*** *2X External mode clocking window.*

Figure 12 is the waveform view that results from this 2X External acquisition, and Figure 13 is the listing of the same data. In the waveform view, the line titled "LA1: Mag_Sample" shows a series of tick marks, each representing 125 ps of time. The total time between any two rising edges of the CK0 signal is 1.625 ns, so the logic analyzer records a valid data state on every 1.625 ns increment of time.

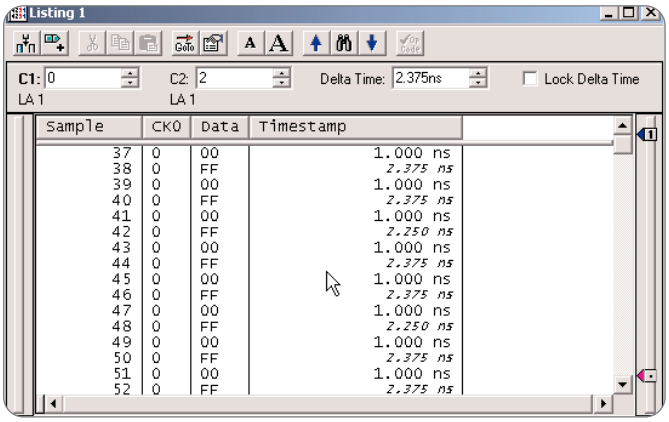
This fast (2X) clocking mode has a special characteristic that must be kept in mind, as the waveform view in Figure 12 shows. The system software places the timestamp of the second sample in the cycle 1 ns after the first sample is taken. This is necessary because the timestamp machine runs at a maximum frequency of 500 MHz (a 2 ns period) and the software must pick a delay that describes when the second edge sample occurred. This value is 1 ns.

2X External, Double Pumped

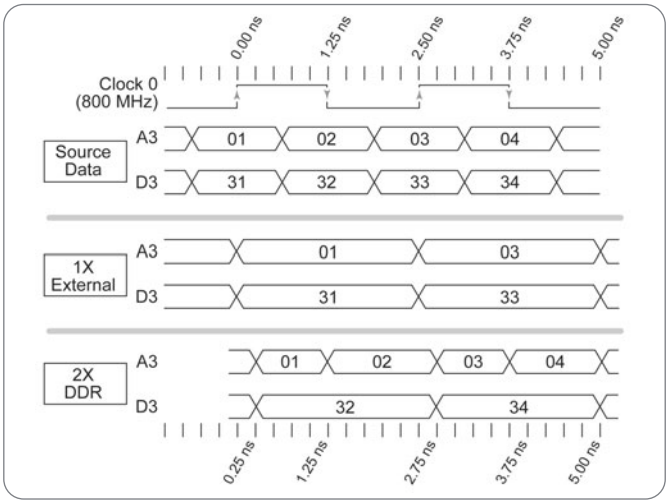
Some devices "double-pump" their data: they drive data on every edge, rising or falling, of a master clock signal. Here again the 2X External mode is the solution. The frequency limit for this mode is 450 MHz, but since the device is double-pumping, the net data rate is 900 Mb/s. Like the basic 2X mode described previously, the system adds 1 ns "separator" increments after the first sample in each cycle. A typical timing scheme for this mode appears in Figure 14.



▶ ***Figure 12.*** *2X External mode acquisition results waveform view.*



▶ ***Figure 13.*** *2X External mode acquisition results listing view.*



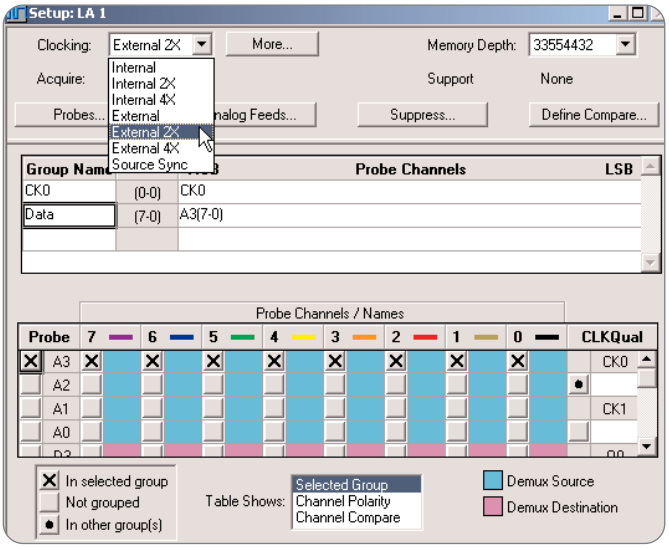
▶ ***Figure 14.*** *2X External "double-pumped" timing.*

As before, the process begins with selecting “External 2X” and assigning the physical connections on the Setup page (Figure 15).

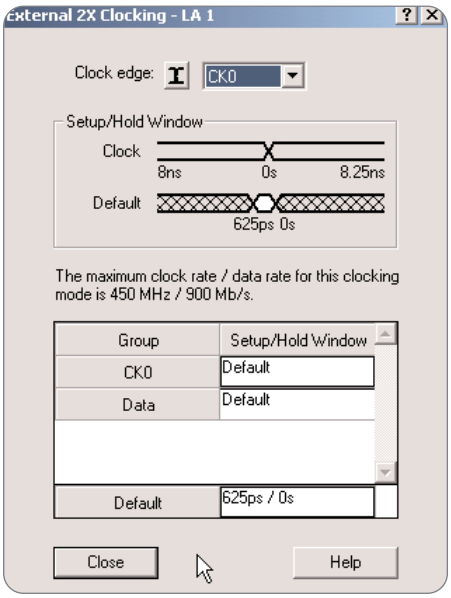
The Clock menu (Figure 16) too is similar to that of the basic 2X mode, except we use the “Clock edge” button to choose the symbol representing a pair of edges. The waveform and listing views, Figures 17 and 18 respectively, summarize the results of the acquisition.

External 4X Clocking

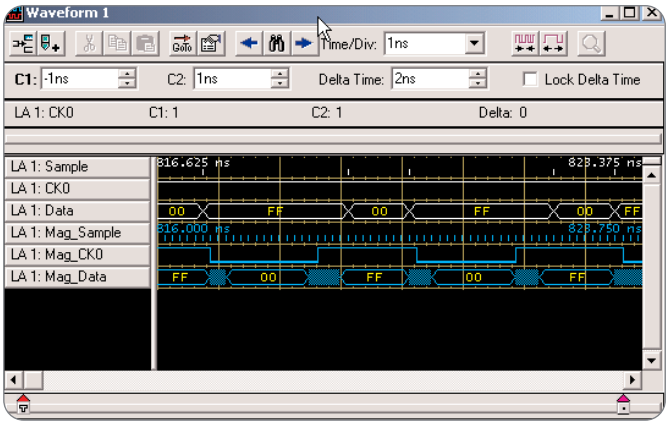
Quad-pumped devices deliver data four times in each SUT cycle. The TLA700 Series provides an External 4X clocking mode that is ideal for this type of device. In addition, it is possible to acquire quad-pumped data using a combination of the basic External (“1X”) mode and demultiplexing. We will cover both approaches here.



► ***Figure 15.*** *2X Double-pumped mode setup page.*



► ***Figure 16.*** *2X Double-pumped mode clock menu.*



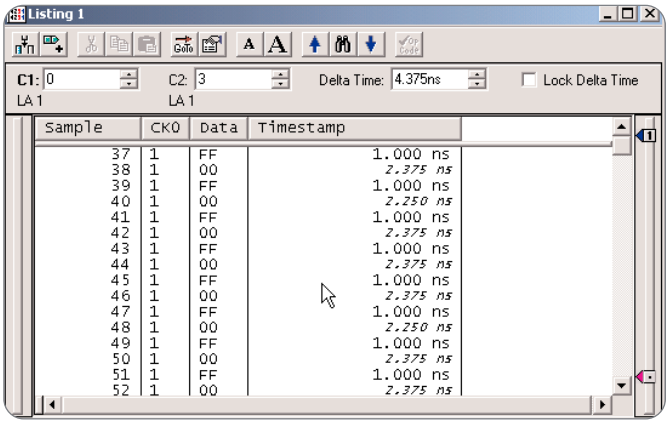
► ***Figure 17.*** *2X Double-pumped mode waveform view.*

Acquiring Quad-Pumped Data Using the External 4X Mode

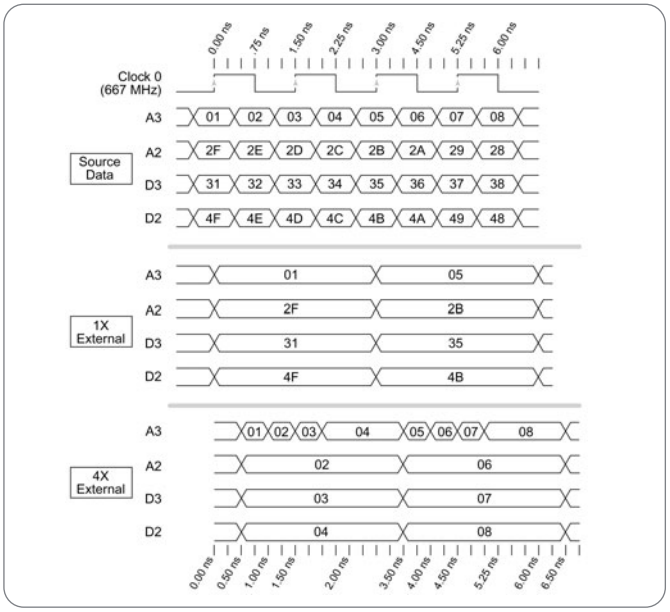
Figure 19 is a conceptual timing diagram for the basic 4X External mode.

As of Version 4.2 TLA Series software, the system displays the 4X data on A3 as follows: the first two samples are evenly spaced at 500 ps intervals; the third sample is placed 500 ps after the second sample. The fourth sample uses up the remaining time in the cycle.

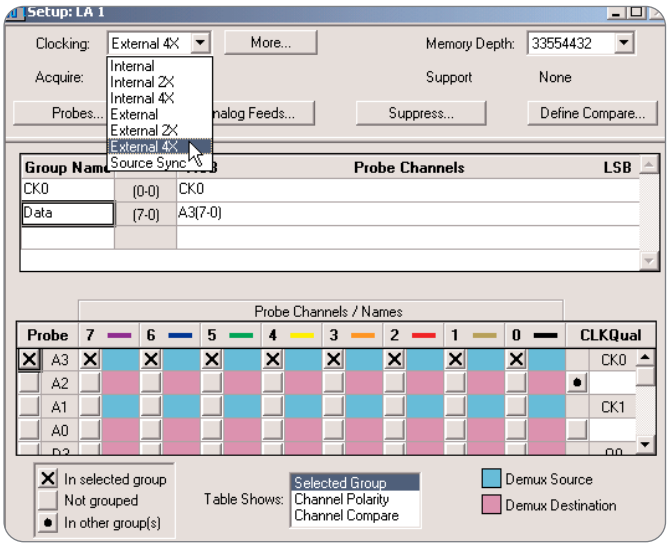
By selecting "External 4X" on the Setup page (Figure 20), you can achieve the highest data rates available from the TLA700 Series logic analyzer—more than 3X the maximum clock rate of the TLA7Axx module; up to 1.25 Gb/s. This mode is well suited to today's high-speed digital communication buses.



▶ ***Figure 18.*** *2X Double-pumped mode listing view.*



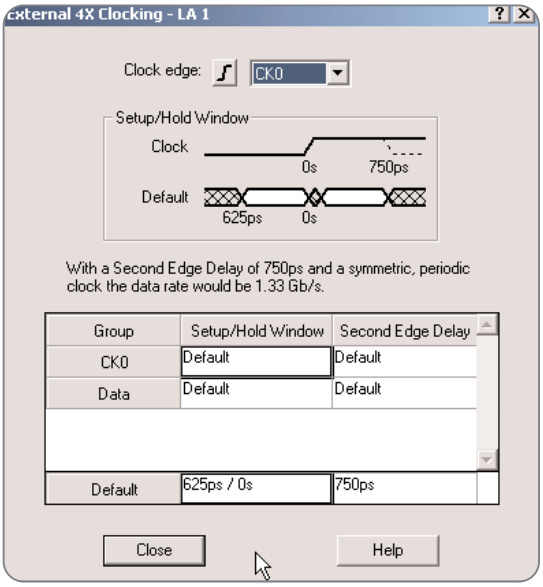
▶ ***Figure 19.*** *4X External timing diagram.*



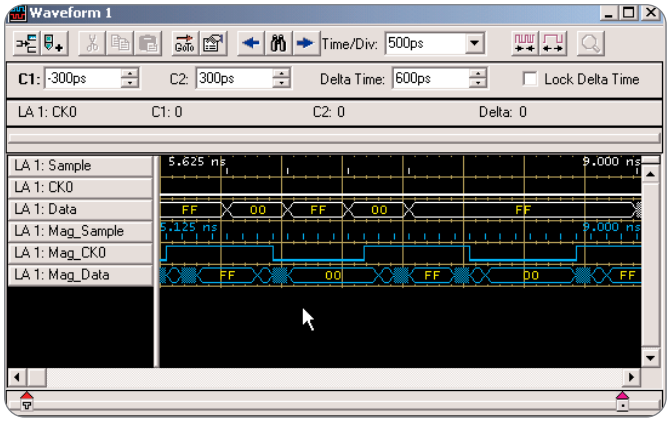
▶ ***Figure 20.*** *4X mode setup page.*

This mode works by sampling twice on each clock edge from the SUT. The normal Setup/Hold parameters dictate sampling on the leading edge of the clock. To capture the data from the trailing edge, you must set a delay value that tells the logic analyzer when to look for the edge. In Figure 21, the "Second Edge Delay" is 750 ps. As this Clock page explains, the theoretical data rate is 1.33 Gb/s. This is a calculated number; note that TLA700 performance beyond 1.25 Gb/s is not guaranteed.

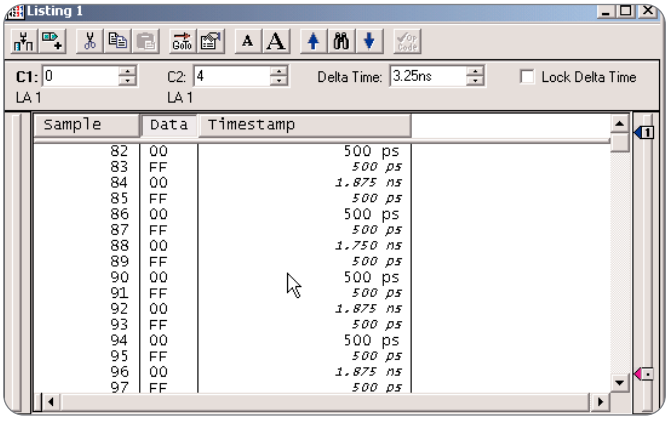
The waveform and list views showing the results of the 4X External mode acquisition are shown in Figures 22 and 23, respectively. In Figure 23, note that the system has again placed "separators" after the first sample in each cycle. In this 4X mode, the system defaults to add 500 ps, between the samples (in contrast to the 1 ns added by both 2X modes).



▶ ***Figure 21.*** *4X mode clocking page.*



▶ ***Figure 22.*** *4X mode waveform view.*



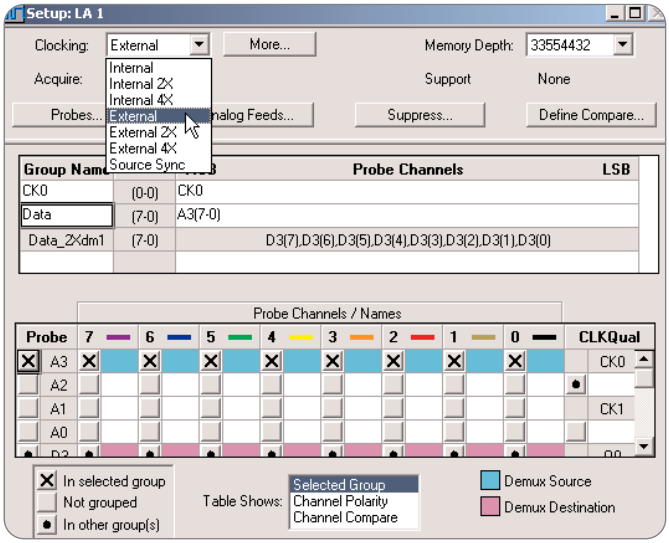
▶ ***Figure 23.*** *4X mode listing view.*

Acquiring Quad-Pumped Data Using the Demultiplexing Method

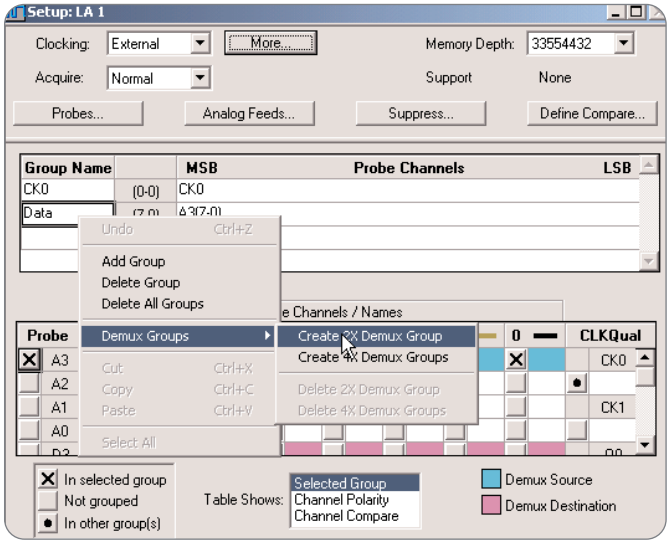
The second method of acquiring data from a quad-pumped SUT doesn't actually use the 4X External mode. Instead, it uses the basic (1X) External mode and demultiplexing techniques to capture four data events per cycle. This mode is preferred when the clock speeds are below 450 MHz. Figure 24 shows the Setup page. Note that "External" is selected here, not "External 4X."

Continuing on the Setup page, right-click the field named "Data" in the Group Names column. This produces a pull-down menu from which you can specify either a 2X or a 4X demux (demultiplex) group, as seen in Figure 25. Choosing "Create 2X Demux Group" sets up the logic analyzer to use a pair of channels on the specified edges, doubling the effective acquisition rate.

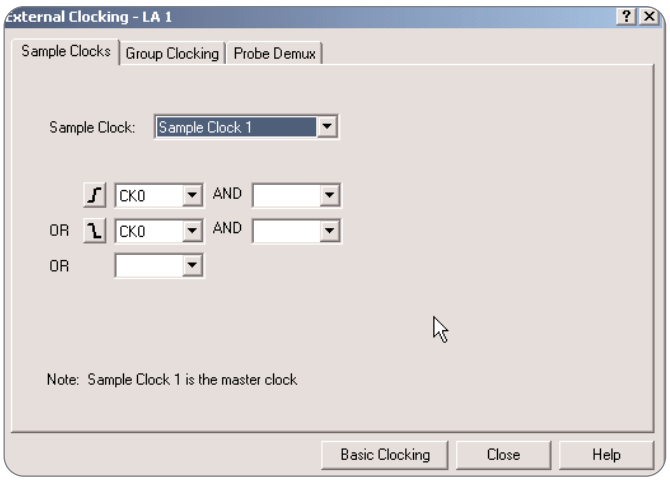
Move to the first tab of the clocking page (Figure 26). CK0 is designated as the master clock, and you must choose a logical OR condition for its edges. Either the rising edge OR the falling edge will clock valid data.



▶ ***Figure 24.*** *Quad pumped mode setup page 1.*



▶ ***Figure 25.*** *Quad pumped mode setup page showing additional menu selections.*

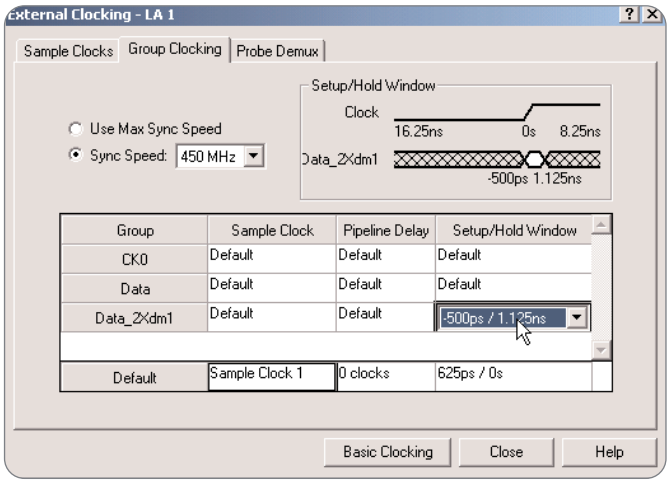


▶ ***Figure 26.*** *Quad pumped mode sample clock page.*

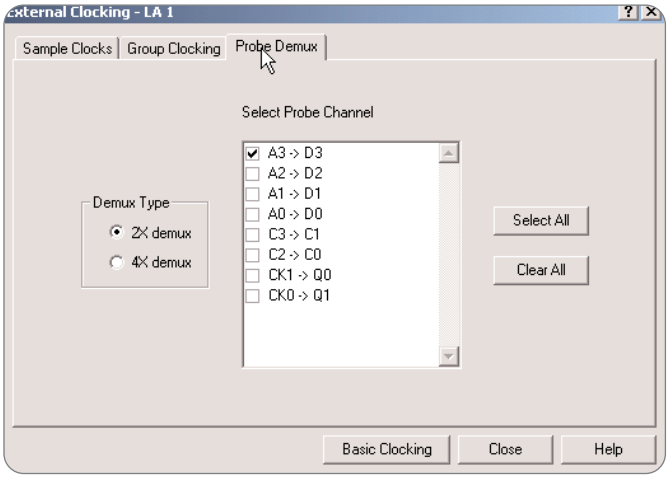
On the Group Clocking tab (Figure 27), it is critical to set up the proper timing on the demux data group (Data_2Xdm1). The Setup/Hold timing setting on this group determines when the logic analyzer looks for the later of the two data samples associated with each edge.

The final step is the Probe Demux tab, shown in Figure 28. Select "2X Demux" (since this is what we specified on the Setup page) and check "A3 › D3" in the "Select Probe Channel" window.

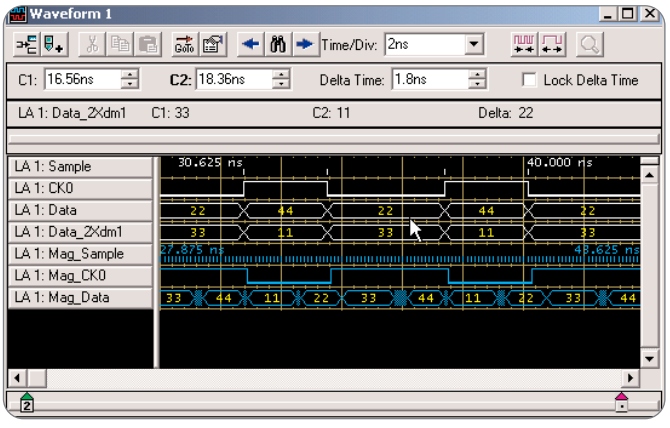
Figures 29 and 30 show the waveform and listing views, respectively, from the quad-pumped data acquisition. On the listing page, note that half of the data resides in the "Data_2xdm1" column, while the other half occupies the "Data" column. This is an arbitrary assignment that does not affect the acquisition outcome. The placement in the columns is entirely dependent on when the logic analyzer acquisition actually starts.



▶ ***Figure 27.*** *Quad-pumped mode group clocking page.*



▶ ***Figure 28.*** *Quad pumped mode probe demux page.*



▶ ***Figure 29.*** *Quad pumped listing page.*

Step-by-Step Application Examples: Source-Synchronous Buses

To capture data from a source synchronous bus, you must use a dedicated source-synchronous acquisition mode. All of the modes discussed up to this point rely on a conventional clock signal to clock data into the logic analyzer. The source synchronous uses dedicated strobe signals instead of, or sometimes in addition to, a normal clock pulse. The TLA700 Series logic analyzer, alone among instruments of its type, can address this need without external interfaces to pre-process the data.

Source synchronous architecture is gaining popularity in digital systems, and designers are likely to encounter it more frequently in the future. For this reason, and because source synchronous acquisition is inherently more complex than other modes, the balance of this document is devoted to two detailed source sync application examples. Specifically, the examples include:

- **Example 1:** acquisition with a master clock, one data strobe, and Return-t0-Zero (RZ) data format.
- **Example 2:** acquisition with a master clock, three data strobes, and Double Data Rate (DDR) data.

Two Kinds Of Source Synchronous Transfers

Before proceeding with an explanation of clocking, it is necessary to understand the differences between Type 1 and Type 2 source synchronous data transfers.

Type 1 buses use data strobes to transfer data, as described in and earlier discussion in this document and illustrated in Figure 1. Some of the leading source synchronous buses today are: AGP (2X, 4X, and 8X); Intel® IA32 front side bus (Pentium® 4); and Intel IA64 front side bus (Itanium®).

Common characteristics of Type 1 source synchronous buses include:

- Data rates between 133 MT/s and 800 MT/s
- Multi-drop
- Bidirectional
- One common-clock domain (for control)
- At least one source-synchronous strobe domain (for address and data)
- Multiple strobe groups per source-synchronous strobe domain
- Undefined skew between strobe groups
- Non-persistent strobes (edges only occur when there is valid data)
- Most Type 1 buses include an explicit bus reset signal.

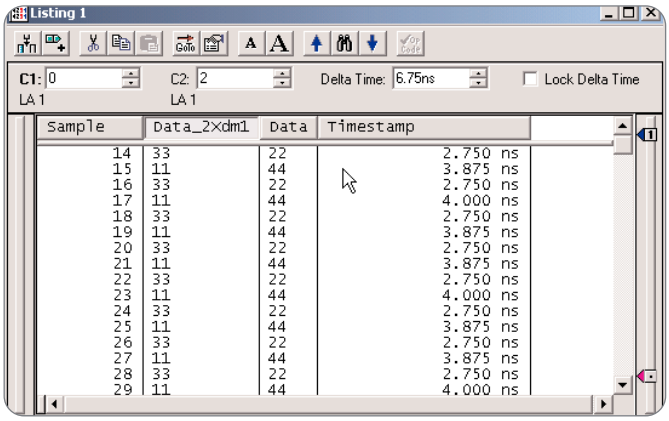
In general, source-synchronous data must be demultiplexed and synchronized with the common-clock data for triggering and analysis. Determining which clock frame to associate with the demultiplexed data is perhaps the biggest challenge when acquiring data from Type 1 buses. Figure 31 depicts some of the variables that can affect the acquisition. Early signals, late signals, skewed data, or jittery strobes can impact the acquisition. In TLA Series logic analyzers, MagniVu acquisition can help resolve these small but important timing deviations.

Type 2 source synchronous transfers take a different approach. There are no strobes, as shown in Figure 32.

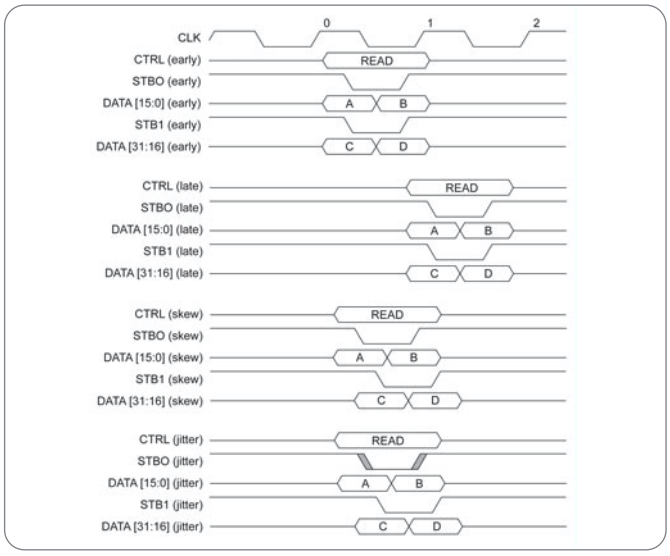
Examples of Type 2 buses include HyperTransport, RapidIO (8- and 16-bit), and POS-PHY4. Common characteristics of Type 2 buses are as follows:

- Data rates ranging from 200 MT/s and 2 GT/s.
- Point-to-point
- Unidirectional
- No separate common clock domain
- Only one source synchronous clock domain
- One or more clock groups
- Undefined skew between clock groups
- Persistent clocks (edges appear with or without valid data)
- No explicit bus reset signal

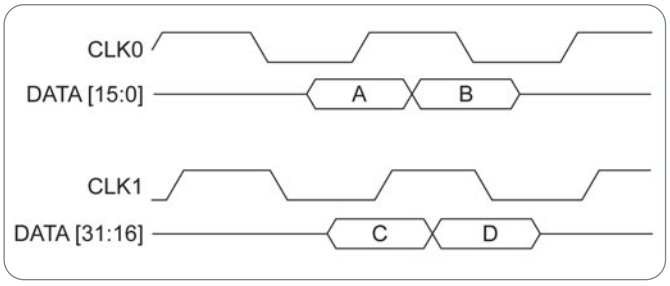
It is necessary to demultiplex and synchronize the source synchronous data across all groups for triggering and analysis. The challenge here, as before is to correctly determine which clock frame to associate with each data pump. With buses that have only one clock group (POS-PHY4 and RapidIO 8-bit, for example) this is not a problem.



▶ ***Figure 30.*** *Quad pumped waveform view.*



▶ ***Figure 31.*** *Timing variations can affect the acquisition and demultiplexing of source synchronous data.*



▶ ***Figure 32.*** *Type 2 source synchronous transfers do not depend on a dedicated strobe.*

In a HyperTransport bus, which has two clock groups, there is no strict specification as to which clock is considered "leading" or "lagging." This opens the possibility of taking data from the front-end FIFOs too early if the lagging clock is the master. If the two clocks are in perfect alignment, the logic analyzer might sample the clock's edge leading on one sample and lagging on another. Figure 33 depicts some of these dual-clock acquisition schemes. Here, the falling edge of CLK1 is the master, and is used as the only contributor to the clock-group-complete circuit.

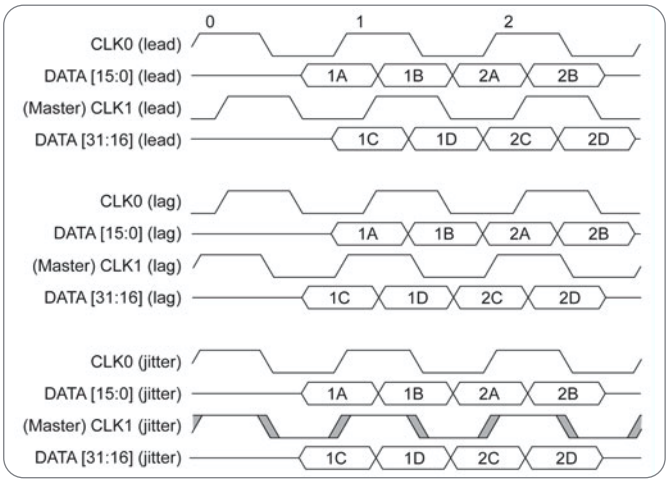
Again, the TLA Series' MagniVu function is a powerful tool for capturing small edge placement variations and determining what is truly leading or lagging.

Source Synchronous Clocking Overview

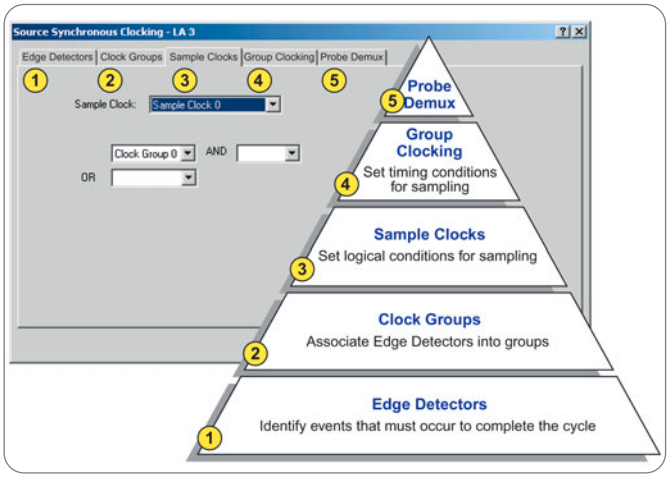
The Source Synchronous clocking setup process has more steps than the 2X and 4X modes discussed earlier. These steps can be viewed as a "pyramid" made up of successive layers of configuration choices (Figure 34).

Setup Screen

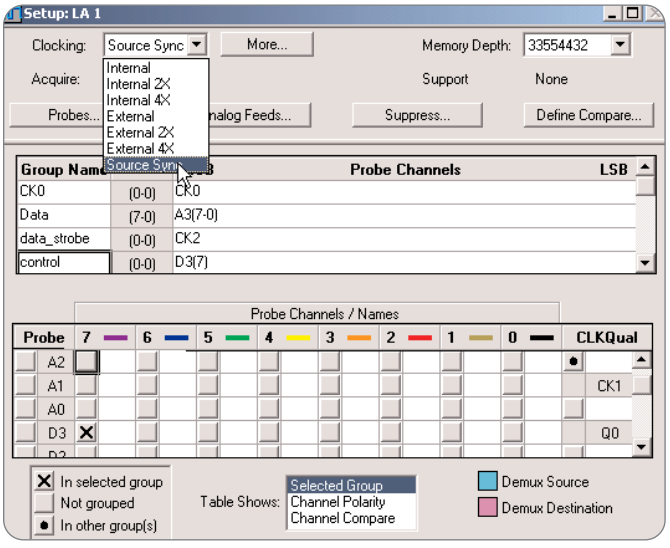
The Setup screen is common to all of the modes and therefore is not shown as part of the Source Sync pyramid. But it is a required step, and Figure 35 shows a Setup page filled out for Source Synchronous acquisition. This page differs from previous Setup pages only in the selection of "Source Sync" on the Clocking pull-down menu, and in the number of signals in the Group Names field.



► ***Figure 33.*** *A dual-clock acquisition using CLK1 as the master.*



► ***Figure 34.*** *Preparing for a source-synchronous acquisition.*



► ***Figure 35.*** *Source-synchronous setup page.*

Edge Detectors Tab

In this example we will be acquiring an AA-55 pattern from a Type 1 source synchronous bus. The data is in a Return to Zero (RZ) format. Figure 36 is a waveform view that includes the MagniVu results acquired at 125 ps resolution (8 GHZ sample rate).

The first step on the pyramid is to assign the Edge Detectors; these are on the left-most tab or the Source Synchronous Clocking menu (Figure 37). Edge Detector 0 is hardwired as the Clock State Machine (CSM) Heartbeat Clock. This is the signal that clocks both the Clock State Machine and the Clock Group Complete sections of the TLA Series Logic Analyzer.

The TLA Series' Clock Group Complete section is key to the source synchronous acquisition. It latches and holds a succession of events, and when a final enabling event occurs, it advances all of the accumulated data.

On the Edge Detectors menu you can select four Edge Detectors, each with four clocks, with rising and falling edges assigned independently of one another. The Validate button is used to verify that the clock definition is valid.

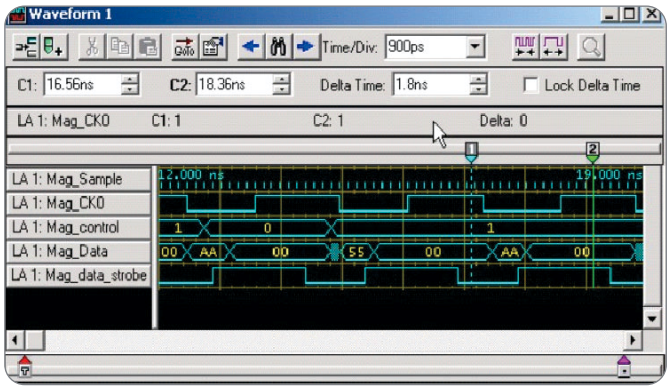
For this example we will assign the rising edge of the main clock signal to Edge Detector Ø, CK0 rising edge. Then we will assign the strobe that enables the completion of a source-synchronous transaction to CK2 rising edge. Now we have configured the basic tools to detect the occurrence of the SUT's main clock signal and strobe.

Clock Groups Tab

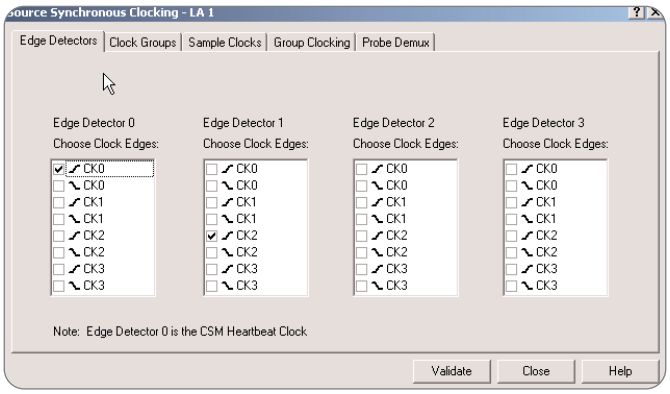
The next menu, Figure 38, sets up the Clock Groups. There are three Clock Groups definitions available; each can contain one or more of the previously-defined Edge Detectors. For this example we will assign Edge Detector 0 to Clock Group 0 and Edge Detector 1 to Clock Group 1, leaving the third Clock Groups unselected.

Other features available in the Clock Groups menu include independent counter/timers, internal and external Clock Group resets. There are some general ground rules for defining Clock Groups:

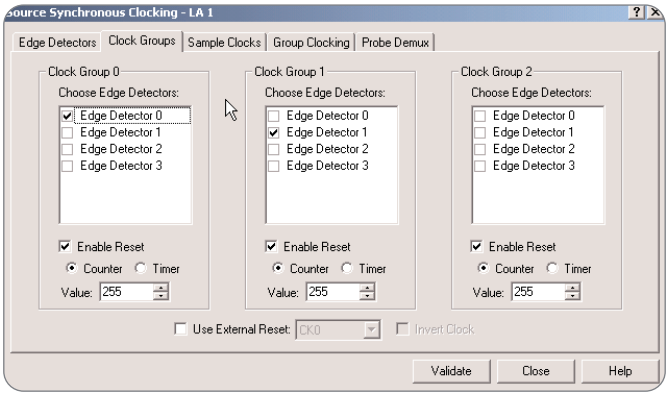
- All of the signals involved in a Clock Group must be of the same frequency
- The master clock for the acquisition must be of equal or greater frequency than the strobes, otherwise the input data pipeline will overflow



▶ ***Figure 36.*** *A source-synchronous waveform acquisition (RZ format).*



▶ ***Figure 37.*** *Edge Detector assignments.*

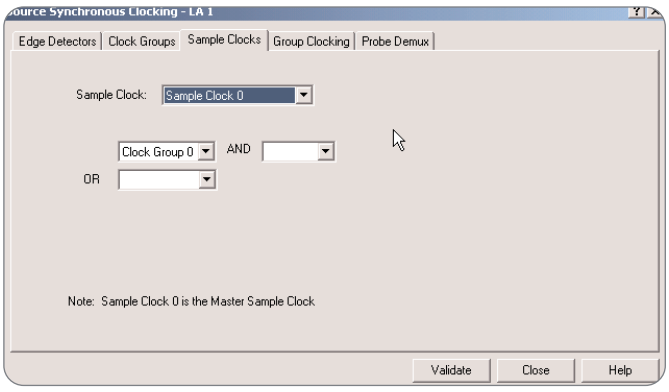


▶ ***Figure 38.*** *Clock Groups selection.*

Sample Clocks Tab

The Sample Clocks submenu (Figure 39) ensures that the logic analyzer samples the data according to the logical conditions that define specific SUT operations. This menu is made up of boolean equations that can be used to qualify the data to meet the differing requirements of Read and Write transactions on a DDR SDRAM bus for example. This Sample Clocks submenu supports up to four sample clocks, each of which can have up to four OR'ed Clock Groups. In turn, each of these may have up to three AND'ed qualifiers. In Figure 35 we have created an entity known as "Sample Clock Ø."

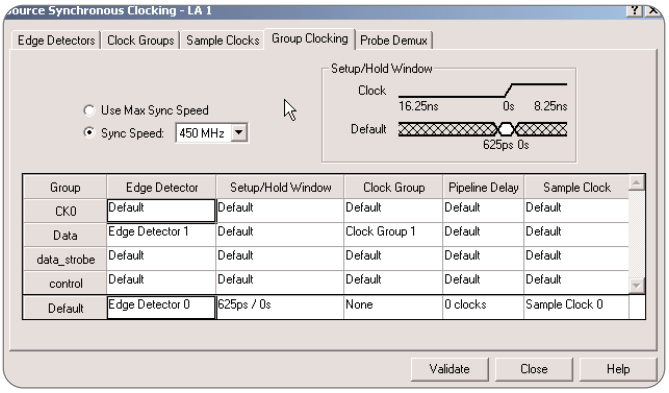
When we fill in this menu as shown in Figure 39, we are telling the logic analyzer to sample when events occur in Clock Group Ø.



► ***Figure 39.*** *Sample Clock equations.*

Group Clocking Tab

The Group Clocking menu (Figure 40—be sure not to confuse this with the Clock Groups menu) is the "workhorse" of the Source Synchronous Clocking setup procedure. It is the point at which all the previous definitions—User Groups, Edge Detectors, Clock Groups, and Sample Clocks—converge. In addition it is the data entry page for Setup/Hold Window and Pipeline Delay figures for all of the user groups (physical signal mappings) defined earlier in the Logic Analyzer Setup menu. You can tell the system to run at its maximum sync speed, or the slower settings of 235 MHz or 120 MHz. In other words, the Group Clocking menu imposes timing parameters on all of the logical conditions we have programmed so far.

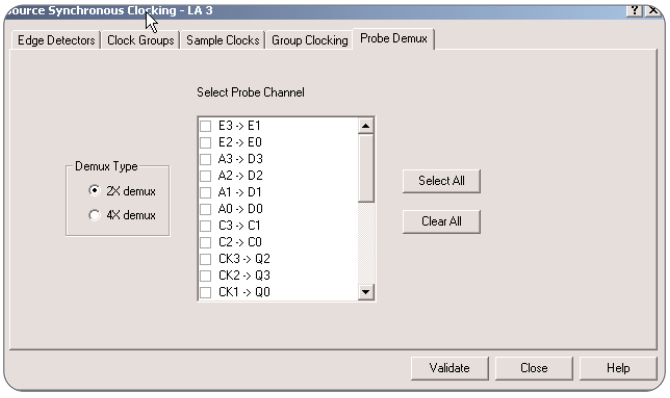


► ***Figure 40.*** *Group Clocking programming.*

Probe Demux Tab

The Probe Demux page is left in its default state (Figure 41)

The captured source synchronous data appears in the listing window (Figure 42). In this example, the strobe latches data on its rising edge. This data is then re-synchronized to the master clock, as you can see in the listing view.



► ***Figure 41.*** *Probe Demux channel selections.*

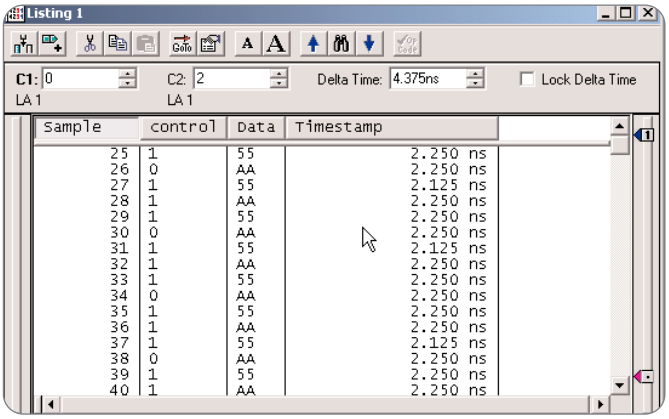
Source Synchronous Acquisition: Example 2

The second source synchronous acquisition approach uses two TLA7XXX modules for the acquisition. We will be acquiring data from a Type 1 source synchronous bus that has a common clock and three data strobes. The timing diagram is shown in Figure 43.

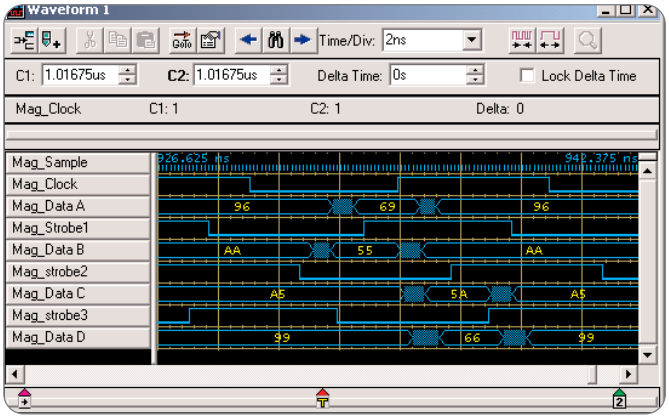
As Figure 43 shows, Data A is clocked in on the rising edge of Clock. Data B is latched on the rising edge of Strobe 1; Data C on the rising edge of Strobe 2, and Data D is latched on the rising edge of Strobe 3. All but Data A are then re-synchronized to the Clock signal. Data A in this example represents a signal that carries control information rather than "Data" in the usual sense of the word and is inherently synchronized to the master clock.

As before, the acquisition starts with the setup process. See Figures 44 and 45, the Setup pages, to understand how the signals are shared among the two acquisition modules.

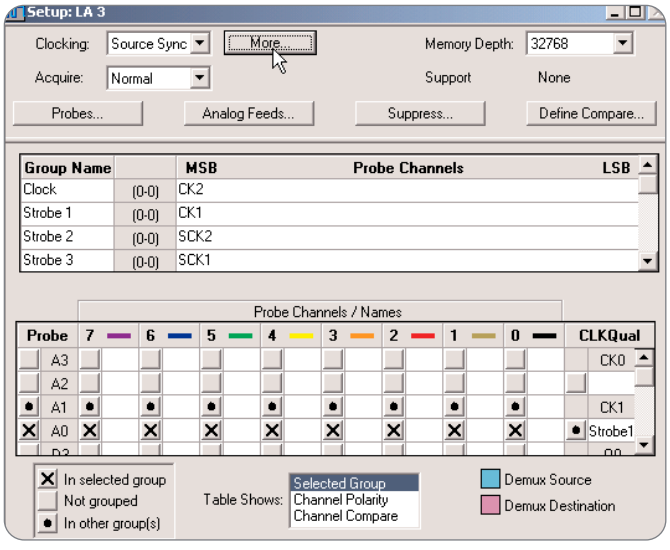
Figure 44 assigns all of the clocking signals. The Master Clock is assigned to CK2, and Strobe 1 goes to CK1. Both of these signals are routed to the master TLA7Axx module. Strobes 2 and 3 go to the slave TLAXXX module and are assigned to SCK2 and SCK1, respectively. Refer again to the timing diagram in Figure 43.



▶ ***Figure 42.*** *Source synchronous listing.*



▶ ***Figure 43.*** *MagniVu-based timing diagram of a source-synchronous bus with a common clock and three strobes.*



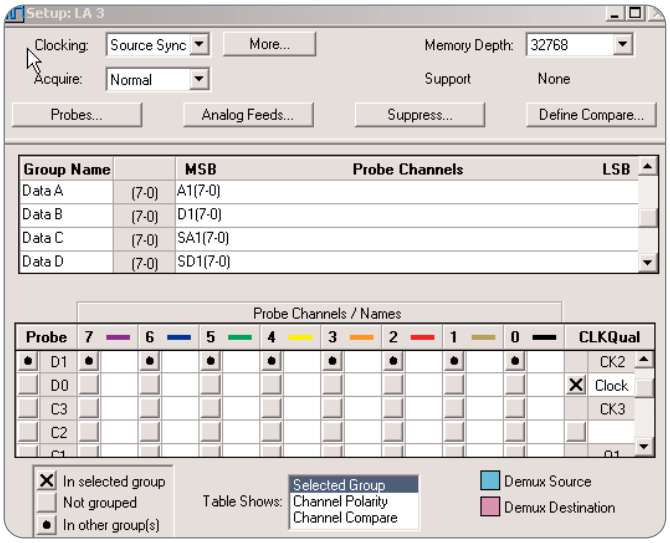
▶ ***Figure 44.*** *Source sync setup page 1.*

Figure 45 assigns all of the Data and Address signals, delivering one address group and one data group to each of the two TLA7Axx modules.

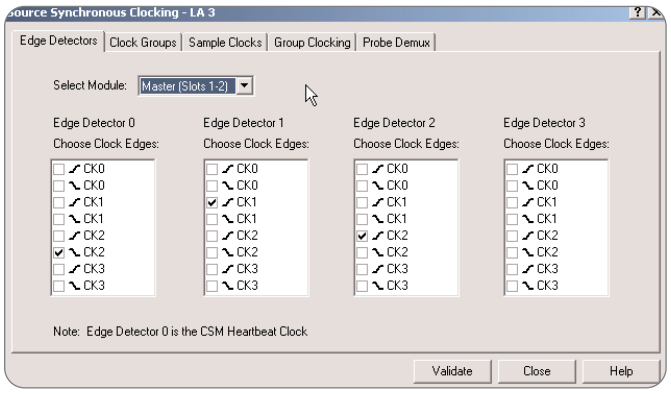
Moving to the Edge Detector assignment menu (Figure 46) for the Master TLA7Axx module, Edge Detector 0 is set to the falling edge of CK2 (the Master Clock signal). This is because the CSM Heartbeat needs to be positioned such that data will be clocked only after all of the strobes have occurred. As it happens, data is clocked on the rising edge of the strobes at about the same time as the falling edge of the Clock, so this falling edge becomes the CSM Heartbeat (remember, Edge Detector 0 is hardwired as the CSM Heartbeat clock).

Also on this menu, Edge Detector 1 is set for the rising edge of Strobe1 to clock in Data B, and Edge Detector 2 is set for the rising edge of Clock to clock in Data A. Note that CK2 is doing double duty: its falling edge acts as the CSM Heartbeat clock and the rising edge clocks in Data A.

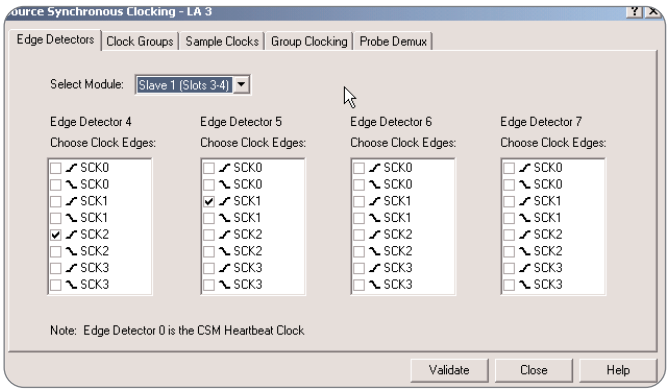
Figure 47 is the second page of Edge Detector assignments. The nomenclature for the individual edges, as in "SCK0," indicates that these signals are going to the slaved TLA7Axx. The master module encompasses detectors 0-3, the first slave module houses detectors 4-7, and so on. In Figure 47, Edge Detector 4 is set for the rising edge of Strobe 2 to clock in Data C, and Edge Detector 5 is set for the rising edge of Strobe to clock in Data D.



▶ ***Figure 45.*** *Source sync setup page 2.*



▶ ***Figure 46.*** *Edge detector page 1.*

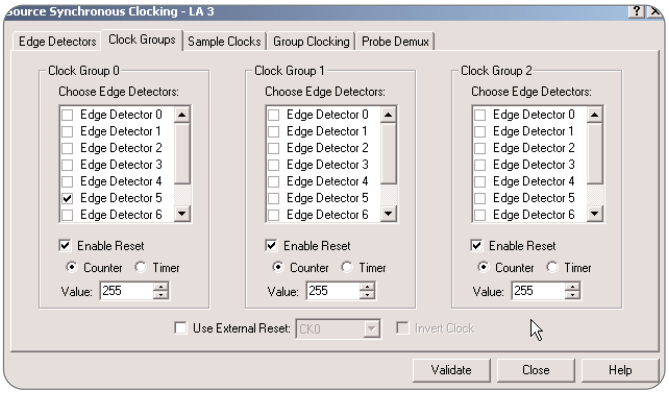


▶ ***Figure 47.*** *Edge detectors page 2.*

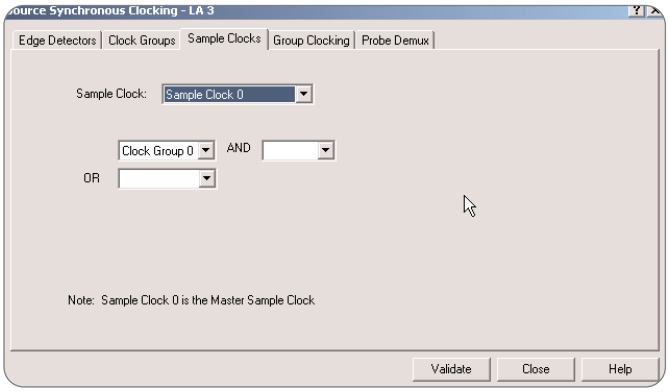
On the Clock Groups menu (Figure 48), Edge Detector 5 is assigned to Clock Group 0. This detector sees the strobe that clocks in Data D, the last edge that happens within the cycle in our SUT's source synchronous bus architecture. Using this detector allows a "clean" startup from a known point in the cycle. Alternatively, if the strobes are not in a known sequence, then using the Timer reset will provide the desired reference point.

Stepping to the next tab, the Sample Clocks menu (Figure 49) can be left in its default state, which assigns Clock Group 0 as the Master Sample Clock.

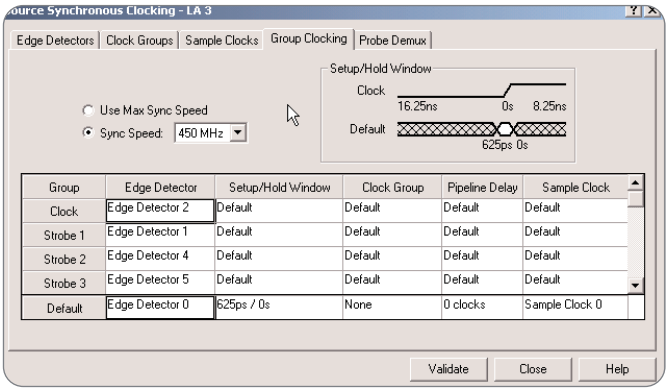
The Group Clocking menu (Figures 50 and 51) brings up the previously-programmed Edge Detector assignments and their associated Groups. Note the correspondence between these assignments and those on the Edge Detector (Figures 46 and 47) and Setup (Figures 44 and 45) menus. Consider Strobe 2 in the Group Clocking menu in Figure 50. On the Setup menu, we assigned Strobe 2 to SCK2. Then we went to the Edge Detectors menu and set Edge Detector 4 to the positive-going edge of SCK2. Thus Edge Detector 4 looks for a rising edge on Strobe 2. This assignment is reflected on the Group Clocking menu in Figure 50, along with the other timing details needed to describe the timing requirements for acquiring the data groups.



▶ ***Figure 48.*** *Clock groups page.*



▶ ***Figure 49.*** *Sample clocks page.*



▶ ***Figure 50.*** *Group clocking page 1.*

As Figure 51 shows, Edge Detector 2 is assigned to Data A; Edge Detector 1 is assigned to Data B; Edge Detector 4 is assigned to Data C; Edge Detector 5 is assigned to Data D.

On the Probe Demux menu (Figure 52), there are no selections. Everything is left in its default state.

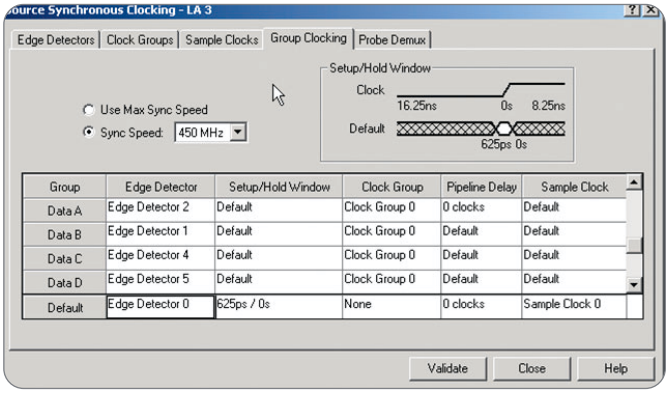
Results of the Source Synchronous Acquisition

Figure 53 is the listing view of the acquisition. It clearly shows that we have correctly captured Type 1 source synchronous data. Data A was captured using the common clock, while Data B, C, and D were captured using strobes 1, 2, and 3.

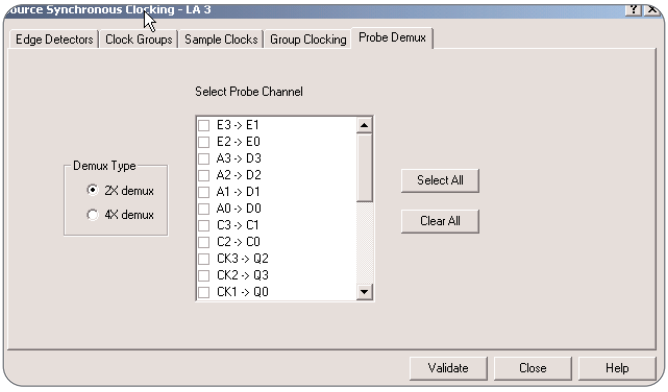
Source Synchronous Notes

The foregoing source-synchronous application examples provide an overview of an important new clocking capability in the TLA Series. When using this mode, some precautions should be observed:

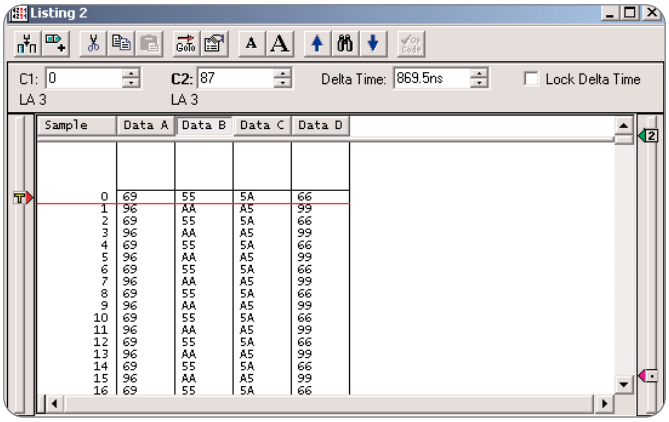
- The source synchronous clocking hardware in the TLA7Axx is designed to wait for the Clock Group Complete (CGC) signal before it clocks the CSM. If the data strobe straddles the master clock—that is, if one edge occurs before the master clock and one edge occurs after the master clock—then that sample will be clocked in on the next edge of the master clock.
- The Strobe edge should not be time-aligned with the master clock, as it may cause the Clock Group Complete signal to shift erratically from one master clock cycle to the next. This will cause the data sample presentation to dither back and forth.
- The 2X synchronous circuit is not used in the source-synchronous clocking. Therefore the separation of any two edges on the same signal must be at least 2.2 ns, equivalent to a maximum clock rate of 450 MHz. If two edges are less than 2.2 ns apart, the second edge will be ignored.



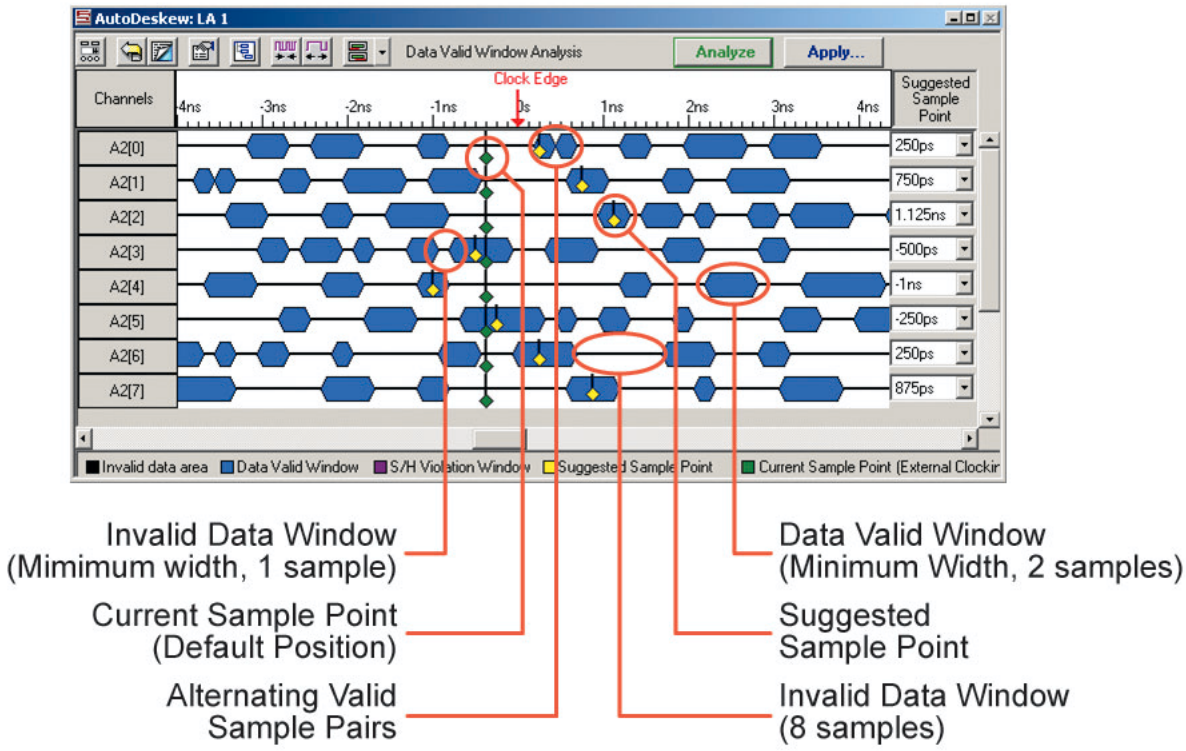
▶ ***Figure 51.*** *Group clocking page 2.*



▶ ***Figure 52.*** *Probe demux page.*



▶ ***Figure 53.*** *Listing view of the source-synchronous acquisition results.*



▶ ***Figure 54.*** *The Auto Deskew Data Valid window identifies sample points, verifies setup/hold settings, and more.*

Auto Deskew Tools

TLA Application Software version 4.3 (and future revisions, when available) includes a new Auto Deskew capability implemented as part of the standard iLink software package. The Auto Deskew feature makes it possible to perform automatic Setup/Hold adjustments and automated Setup/Hold violations on the system under test (SUT). Auto Deskew supports advanced TLA custom clocking as well as the standard clocking configurations discussed in this document. As a component of the TLA Application Software, Auto Deskew uses the standard "Windows" user interface with its familiar look and feel.

How Does Auto Deskew Work?

Auto Deskew looks for two successive MagniVu bins with equal values stored in both. If such a pairing is found, then by definition the signal has a stable valid data window equal to the MagniVu timing resolution, which in the case of the TLA7Axx acquisition module is 125 ps. Note, however, that the minimum valid data window for the module is 750 ps.

Auto Deskew works on a per-channel basis and does not change the threshold value. It runs from a selected user-defined range relative to a user-determined clock definition.

Using Auto Deskew To Acquire Complex Bus Signals

The Auto Deskew feature is a valuable analysis tool that delivers fast answers about critical timing issues in complex bus signals. It can:

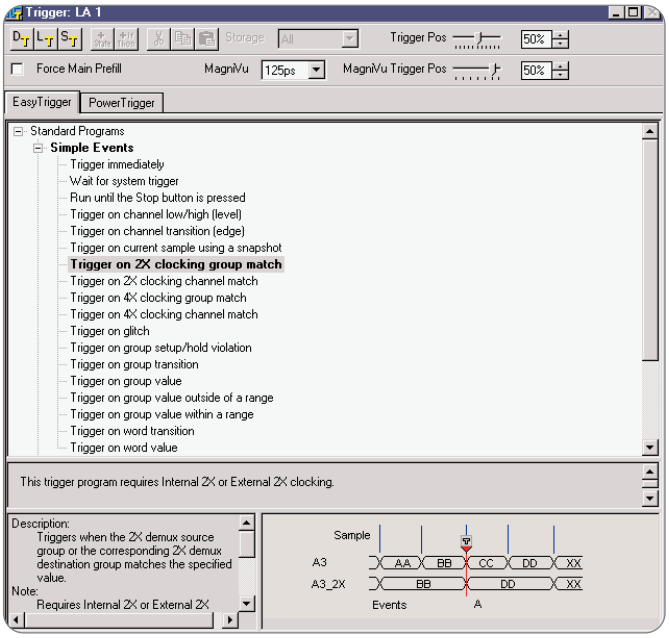
- Look for "any" valid data window on a bus.
- Identify, relative to a strobe, a valid data window for a data group.
- Determine whether a clock rather than a strobe can be used as the master reference clock.
- Deskew a data group across merged module boundaries.
- Help verify setup/hold settings in a custom setup file.

The complete Auto Deskew Data Valid window is depicted in Figure 54. Note that setup/hold violation window placement, though not shown here, is also included where applicable.

The Auto Deskew Data Valid Window analysis page helps you gain an overall understanding of the behavior of today's complex buses. Once you have a grasp of these timing nuances, you will be able to apply the advanced clocking capabilities built into the TLA7Axx module family to capture source synchronous data "straight up," with no need for a pre-processor.

EasyTrigger

Tektronix extends the triggering capabilities of its logic analyzers with a powerful triggering feature called EasyTrigger. This simplified trigger setup menu includes numerous presets, among them triggers for 2X and 4X internal and external clocking modes. Figure 55 shows an example of a triggering on a 2X clocking group match. When you select trigger program in EasyTrigger, the window displays a complete description of your selection as well as a graphical timing diagram of the trigger selection. With EasyTrigger, preparation for an acquisition, even a complex one, is faster and less prone to errors.



▶ ***Figure 55.*** *Tektronix EasyTrigger menu.*

Summary

Logic analyzers have been and continue to be the tool of choice for digital debug of computer, communication and network elements. To increase the data throughput in digital systems, innovative data transfer techniques have been implemented. These techniques include: increasing the basic clock and data speed, sending the data differentially, reducing signal swing amplitude, transferring data multiple times in one clock cycle and sending the data in a source synchronous format.

In order to capture the digital data from the buses implementing these transfer attributes, it is necessary to use an advanced logic analysis tool that can capture these types of buses without the need for a front end "pre-processor" to manipulate—and possibly distort—the data.

The new Tektronix TLA7Axx logic analyzer module has the clocking features to capture data buses that implement these faster data transfer techniques. The tools to handle high speed synchronous clocks, and capture multiplexed buses and source synchronous data transfers are built in to this advanced logic analyzer. This is one logic analyzer you can't live without in today's high-speed digital world!

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